[CONTROL CHIP FOR ACCELERATING MEMORY ACCESS AND METHOD OF OPERATING THE SAME]

Abstract of Disclosure

A control chip for accelerating the memory access and a method of operating the same is disclosed. The disclosed control chip receives a first address strobe (ADS) signal, a request signal, and an address bus signal from the CPU. A second ADS signal will be promptly issued if the selection phase of the request signal is either a memory read signal or a memory write signal and the address phase of the address bus signal indicates an effective memory address. Thereafter the second ADS signal is converted to a third ADS signal referring to the memory clocks. A memory control signal will be issued if no zero-length signal is suggested in length phase of the request signal and in the byte enable phase of the address bus signal. Computer system performances will be significantly upgraded since the third ADS signal is issued one cycle advanced than conventional approaches.

Figures